REMARKS

Claims 1 through 108 are currently pending in the application.

This amendment is in response to the Office Action of January 5, 2004.

Objection to Priority Claim

The first paragraph of the specification has been amended to set forth the priority claim for the application as well as related applications to the present application and their relationship thereto.

Objection to Declaration

The declaration is objected to for failing to have a common inventor with the instant application. Applicants have attached a Supplemental Declaration in accordance with the Examiner's request.

Double Patenting Rejection Based on U.S. Patent 5,907,492

Claims 1 through 108 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 through 26 of U.S. Patent 5,907,492.

Claims 1 through 108 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 through 35 of U.S. Patent 6,363,295.

Claims 1 through 108 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 through 35 of U.S. Patent 6,553,276.

Claims 1 through 108 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 through 20 of copending Application No. 10/401,209.

In order to avoid further expenses and time delay, Applicants elect to expedite the prosecution of the present application by filing a terminal disclaimer to obviate the double patenting rejections in compliance with 37 C.F.R. §1.321 (b) and (c). Applicants' filing of the terminal disclaimers should not be construed as acquiescence of the Examiner's double patenting or obviousness-type double patenting rejections. Attached are the terminal disclaimers and

accompanying fees.

35 U.S.C. § 101 Double Patenting Rejection

Claim 38 is rejected under 35 U.S.C. § 101 as claiming the same invention as that of claim 34 of prior U.S. Patent 6,363,295 (hereinafter referred to as the `295 patent). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants assert that a reliable test for statutory double patenting under 35 U.S.C. § 101 is whether a claim in the application can be literally infringed without literally infringing a corresponding claim in the patent. Is there an embodiment of the invention that falls within the scope of one claim, but not the other? If there is such an embodiment of the invention, then identical subject matter is not defined by both claims and statutory double patenting under 35 U.S.C. § 101 does not exist. *In re Vogel,* 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

Applicants assert that no statutory double patenting under 35 U.S.C. § 101 exists between the embodiment of the presently claimed invention of presently amended independent claim 38 of the present application and corresponding independent claim 34 of the `295 patent because different embodiments of the inventions are being claimed ins such claims. For instance, the embodiment of the invention set forth in presently amended independent claim 38 of the present application clearly has an element of the presently claimed invention calling for "diverting semiconductor devices identified as good but unrepairable by the accessed data to one of use in other semiconductor device manufacturing processes and discarding the semiconductor devices identified as good but unrepairable" whereas the embodiment of the invention set forth in corresponding independent claim 34 of the `295 patent does not. Therefore, since different embodiments of the inventions are being claimed between presently amended independent claim 38 of the present application and corresponding claim 34 of the `295 patent, no statutory double patenting under 35 U.S.C. § 101 exists therebetween. Accordingly, presently amended independent claim 38 and dependent claim 39 therefrom are allowable.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on Beffa (U.S. Patent 5,927,512)

Claims 1, 2, 7 through 11, 40, 41, 46, 47 and 50 through 53 are rejected under 35 U.S.C. § 102(e) as being anticipated by Beffa (U.S. Patent 5,927,512). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants assert that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants assert that presently amended independent claims 1 and 40 are not anticipated by the Beffa reference under 35 U.S.C. § 102 because the Beffa reference does not identically describe, either expressly or inherently, each and every element of the presently claimed invention in as complete detail as is contained in the claims.

Turning to the cited prior art, the Beffa reference is directed to a method for sorting integrated circuit devices having substantially unique identification codes, such as a fuse ID, by automatically reading the ID code of each of the IC devices and sorting the IC devices in accordance with their automatically read ID codes. The fuse ID may identify a wafer lot ID, the week the IC's were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID.

Applicants assert that the Beffa reference does not and cannot describe, either expressly or inherently, each and every element of the Applicants presently claimed inventions of presently amended independent claims 1 and 40 calling for "storing data in association with the identification code of each semiconductor device of the plurality identifying manufacturing procedures each semiconductor device has undergone", "automatically reading the identification code of each semiconductor device", "accessing the data stored in association with the identification code of each semiconductor device", and "storing data in association with the identification code of each semiconductor device of the semiconductor devices identifying manufacturing procedures the semiconductor device has undergone".

In contrast to the elements of the presently claimed inventions of independent claims 1 and 40, the Beffa reference describes either explicitly or inherently, to a method for sorting integrated circuit devices having substantially unique identification codes, such as a fuse ID, by automatically reading the ID code of each of the IC devices and sorting the IC devices in accordance with their automatically read ID codes where the fuse ID either identifies a wafer lot ID, identifies the week the IC's were fabricated, identifies a wafer ID, identifies a die location on the wafer, and/or identifies a fabrication facility ID. Such are not the elements of the presently claimed inventions of presently amended independent claims 1 and 40 wherein the data stored is based on storing data in association with the identification code of each semiconductor device . . . identifying manufacturing procedures <u>each</u> semiconductor device has undergone", "automatically reading the identification code of each semiconductor device", "accessing the data stored in association with the identification code of each semiconductor device", and "storing data in association with the identification code of each semiconductor device <u>of the semiconductor devices</u> identifying manufacturing procedures the semiconductor device has undergone".

Accordingly, presently amended independent claims 1 and 40 are allowable as well as dependent claims 2, 7 through 11, 41, 46, 47, and 50 through 53 therefrom.

<u>Anticipation Rejection Based on Beffa (U.S. Patent 5,915,231)</u>

Claims 1, 2, 6 through 11, 17 through 27, 40, 41, 45 through 47, 50 through 53, 59 through 63, 66 through 68, 73, 74, 80 through 83, 86 through 88, 93, 100 through 103, 106 and 107 are rejected under 35 U.S.C. § 102(e) as being anticipated by Beffa (U.S. Patent 5,915,231). Applicants respectfully traverse this rejection, as hereinafter set forth.

Again Applicants assert that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants assert that presently amended independent claims 1, 18, 25, 40, 60, 80, and 100 are not anticipated by the Beffa reference under 35 U.S.C. § 102 because the Beffa reference does not identically describe, either expressly or inherently, each and every element of the presently claimed invention in as complete detail as is contained in the claims.

Turning to the cited prior art, the Beffa reference is directed to a method for manufacturing IC devices from wafers including providing the wafers and fabrication IC's on the wafers. The IC's include substantially unique identification codes, such as a fuse ID, by automatically reading the ID code of each of the IC devices and sorting the IC devices in accordance with their automatically read ID codes. The fuse ID may identify a wafer lot ID, the week the IC's were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID.

Applicants assert that the Beffa reference does not and cannot describe, either expressly or inherently, each and every element of the Applicants presently claimed inventions of presently amended independent claims 1 and 40 calling for "storing data in association with the identification code of each semiconductor device of the plurality identifying manufacturing procedures ~~the~~ each semiconductor device has undergone", "automatically reading the identification code of each semiconductor device", "accessing the data stored in association with the identification code of each semiconductor device", "causing each semiconductor device of the plurality on each of the wafers to store a substantially unique identification code", "storing data in association with the identification code of each semiconductor device of the plurality that identifies manufacturing procedures ~~the~~ each semiconductor device has undergone", "separating each semiconductor device of the plurality on each of the wafers from its wafer to form one semiconductor ~~device~~ die of a plurality of semiconductor ~~dice~~devices", "assembling each semiconductor device into a semiconductor device assembly", "automatically reading the identification code associated with each semiconductor device", "accessing the data stored in association with the identification code associated with each semiconductor device", and "storing data in association with the identification code of each semiconductor device of the semiconductor devices identifying manufacturing procedures the semiconductor device has

undergone" as well as similar elements of the claimed inventions of independent claims 18, 25, 60, 80, and 100.

In contrast to the elements of the presently claimed inventions of independent claims 1, 18, 25, 40, 60, 80, and 100, the Beffa reference describes either explicitly or inherently, to a method for sorting integrated circuit devices having substantially unique identification codes, such as a fuse ID, by automatically reading the ID code of each of the IC devices and sorting the IC devices in accordance with their automatically read ID codes where the fuse ID either identifies a wafer lot ID, identifies the week the IC's were fabricated, identifies a wafer ID, identifies a die location on the wafer, and/or identifies a fabrication facility ID. Such are not the elements of the presently claimed inventions of presently amended independent claims 1 and 40 wherein the data stored is based on storing data in association with the identification code of each semiconductor device . . . identifying manufacturing procedures each semiconductor device has undergone", "automatically reading the identification code of each semiconductor device", "accessing the data stored in association with the identification code of each semiconductor device", "storing data in association with the identification code of each semiconductor device of the semiconductor devices identifying manufacturing procedures the semiconductor device has undergone", etc as well as similar elements of independent claims. In Applicants' claimed inventions, the data in the identification code is based on manufacturing procedures where the cited prior art is not.

Accordingly, presently amended independent claims 1, 18, 25, 40, 60, 80, and 100 are allowable as well as dependent claims 2, 6 through 11, 17 through 27, 41, 45 through 47, 50 through 53, 59, 61 through 63, 66 through 68, 73, 74, 81 through 83, 86 through 88, 93, 102, 103, 106, and 107 therefrom.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on Shils et al. (U.S. Patent 4,510,673)

Claims 1, 2, 6, 8, 10, 17 through 19, 25, 26, 40, 41, 45, 47, 49, 50, 59 through 61, 65, 80, 81, 85, 100, 101 and 105 are rejected under 35 U.S.C. § 102(b) as being anticipated by Shils et

al. (U.S. Patent 4,510,673). Applicants respectfully traverse this rejection, as hereinafter set forth.

Again Applicants assert that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants assert that presently amended independent claims 1, 18, 25, 40, 60, 80, and 100 are not anticipated by the Shils et al. reference under 35 U.S.C. § 102 because the Shils et al. reference does not identically describe, either expressly or inherently, each and every element of the presently claimed invention in as complete detail as is contained in the claims.

Turning to the cited prior art, the Shils et al. reference is directed to a system of identifying each chip with identification data that is both human and machine readable using a laser written semiconductor chip identification to scribe an identification code on the back of each chip. The chip identification utilizes a scribing tool to provide positive identification and test data relative to individual chips. Such data includes unique manufacturing codes which identify wafer type, part number and production controls, such as the production line, date of manufacture and the like. Additionally, data generated during testing is used to provide additional written data.

Applicants assert that the Shils et al. reference does not and cannot describe, either expressly or inherently, each and every element of the Applicants presently claimed inventions of presently amended independent claims 1 and 40 calling for "storing data in association with the identification code of each semiconductor device of the plurality identifying manufacturing procedures ~~the~~ each semiconductor device has undergone", "automatically reading the identification code of each semiconductor device", "accessing the data stored in association with the identification code of each semiconductor device", "causing each semiconductor device of the plurality on each of the wafers to store a substantially unique identification code", "storing data in association with the identification code of each semiconductor device of the plurality that identifies manufacturing procedures ~~the~~ each semiconductor device has undergone", "separating

each semiconductor device of the plurality on each of the wafers from its wafer to form one semiconductor ~~device~~ die of a plurality of semiconductor ~~dice~~devices", "assembling each semiconductor device into a semiconductor device assembly", "automatically reading the identification code associated with each semiconductor device", "accessing the data stored in association with the identification code associated with each semiconductor device", and "storing data in association with the identification code of each semiconductor device of the semiconductor devices identifying manufacturing procedures the semiconductor device has undergone" as well as similar elements of the claimed inventions of independent claims 18, 25, 60, 80, and 100.

In contrast to the elements of the presently claimed inventions of independent claims 1, 18, 25, 40, 60, 80, and 100, the Shils et al. reference describes either explicitly or inherently, to a method for identifying each chip with identification data that is both human and machine readable using a laser code scribed on the back of each chip where such data includes unique manufacturing codes which identify wafer type, part number and production controls, such as the production line, date of manufacture and the like. Additionally, data generated during testing is used to provide additional written data. Such are not the elements of the presently claimed inventions of presently amended independent claims 1, 18, 25, 40, 60, 80, and 100wherein the data stored is based on storing data in association with the identification code of each semiconductor device . . . identifying manufacturing procedures each semiconductor device has undergone", "automatically reading the identification code of each semiconductor device", "accessing the data stored in association with the identification code of each semiconductor device", "storing data in association with the identification code of each semiconductor device of the semiconductor devices identifying manufacturing procedures the semiconductor device has undergone", etc. In Applicants' claimed inventions, the data in the identification code is based on manufacturing procedures where the cited prior art is not.

Accordingly, presently amended independent claims 1, 18, 25, 40, 60, 80, and 100 are allowable as well as dependent claims 2, 6 through 11, 17 through 27, 41, 45 through 47, 50 through 53, 59, 61 through 63, 66 through 68, 73, 74, 81 through 83, 86 through 88, 93, 102, 103, 106, and 107 therefrom.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Shils et al. (U.S. Patent 4,510,673)

Claims 3, 11 and 53 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shils et al. (U.S. Patent 4,510,673). Applicants respectfully traverse this rejection, as hereinafter set forth. Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants further submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Applicants assert that the Shils et al. reference does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of independent claims 1 and 40 because the Shils et al. reference does not teach or suggest all of the claim limitations of such independent claims and the Shils et al. reference does not contain any the suggestion whatsoever for any modification thereto or any reasonable expectation of success for any modification thereto.

Again turning to the cited prior art, the Shils et al. reference is directed to a method for identifying each chip with identification data that is both human and machine readable using a laser code scribed on the back of each chip where such data includes unique manufacturing codes which identify wafer type, part number and production controls, such as the production line, date of manufacture and the like. Additionally, data generated during testing is used to provide additional written data.

Applicants assert that the Shils et al. reference does not and cannot teach or suggest the claim limitations of independent claims 1 and 40 calling for "storing data in association with the identification code of each semiconductor device of the plurality identifying manufacturing

procedures ~~the~~ each semiconductor device has undergone", "automatically reading the identification code of each semiconductor device", "accessing the data stored in association with the identification code of each semiconductor device", "causing each semiconductor device of the plurality on each of the wafers to store a substantially unique identification code", "storing data in association with the identification code of each semiconductor device of the plurality that identifies manufacturing procedures ~~the~~ each semiconductor device has undergone", "separating each semiconductor device of the plurality on each of the wafers from its wafer to form one semiconductor ~~device~~ die of a plurality of semiconductor ~~dice~~devices", "assembling each semiconductor device into a semiconductor device assembly", "automatically reading the identification code associated with each semiconductor device", "accessing the data stored in association with the identification code associated with each semiconductor device", and "storing data in association with the identification code of each semiconductor device of the semiconductor devices identifying manufacturing procedures the semiconductor device has undergone".

In contrast to the claim limitations of the presently claimed inventions of independent claims 1 and 40, the Shils et al. reference teaches or suggests a method for identifying each chip with identification data that is both human and machine readable using a laser code scribed on the back of each chip where such data includes unique manufacturing codes which identify wafer type, part number and production controls, such as the production line, date of manufacture and the like. Additionally, data generated during testing is used to provide additional written data. Such are not the elements of the presently claimed inventions of presently amended independent claims 1 and 40 wherein the data stored is based on storing data in association with the identification code of each semiconductor device . . . identifying manufacturing procedures each semiconductor device has undergone", "automatically reading the identification code of each semiconductor device", "accessing the data stored in association with the identification code of each semiconductor device", "storing data in association with the identification code of each semiconductor device of the semiconductor devices identifying manufacturing procedures the semiconductor device has undergone", etc. In Applicants' claimed

inventions, the data in the identification code is based on manufacturing procedures where in the cited prior art Shils et al. reference the identification code is not.

Further, Applicants assert that there is no suggestion whatsoever in the Shils et al. reference for any modification thereof or the success for any modification thereof to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of independent claims 1 and 40. Applicants assert that the only suggestion for any modification of the Shils et al. reference is solely Applicants' disclosure, not the cited prior art. Any such basis of a rejection using Applicants' disclosure is neither within the ambit nor the purview of 35 U.S.C. § 103 and, clearly, improper.

Accordingly, presently amended independent claims 1 and 40 are allowable as well as dependent claims 3, 11, and 53 therefrom.

Obviousness Rejection Based on Beffa (U.S. Patent 5,915,231) in view of Vu et al. (U.S. Patent 5,256,562)

Claims 68 through 72 and 88 through 92 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Beffa (U.S. Patent 5,915,231) in view of Vu et al. (U.S. Patent 5,256,562). Applicants respectfully traverse this rejection, as hereinafter set forth.

Again Applicants assert that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Applicants assert that any combination of the Beffa reference and the Vu et al. reference does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of independent claims 60 and 80 because any combination of the Beffa reference and the Vu et al. reference does not teach or suggest all the claim limitations of the

claimed invention. Further, any rejection of the claimed inventions of independent claims 60 and 80 based upon any combination of the cited prior art would be a hindsight reconstruction of the claimed inventions based solely upon Applicants' disclosure, not any suggestion in the cited prior art .

Again turning to the cited prior art, the Beffa reference is directed to a method for manufacturing IC devices from wafers including providing the wafers and fabrication IC's on the wafers. The IC's include substantially unique identification codes, such as a fuse ID, by automatically reading the ID code of each of the IC devices and sorting the IC devices in accordance with their automatically read ID codes. The fuse ID may identify a wafer lot ID, the week the IC's were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID.

The Vu et al. reference relates to the formation of arrays of thin film transistors on silicon substrates and the dicing a tiling of such substrates for transfer to a common module body.

Applicants assert that any combination of the Beffa reference and the Vu et al. reference does not and cannot teach or suggest all the claim limitations of Applicants presently claimed inventions of presently amended independent claims 60 and 80 calling for "storing data in association with the identification code of each semiconductor device that identifies manufacturing procedures ~~the~~ each semiconductor device has undergone", "accessing the data stored in association with the identification code associated with the at least one semiconductor device", "storing data in association with the identification code of the at least one semiconductor device identifying manufacturing procedures the at least one semiconductor device has undergone", and "accessing the data stored in association with the identification code associated with the at least two semiconductor devices".

In contrast to the claim limitations of the presently claimed inventions of independent claims 60 and 80, any combination of the Beffa reference and the Vu et al. reference solely teaches or suggests a method for sorting integrated circuit devices having substantially unique identification codes, such as a fuse ID, by automatically reading the ID code of each of the IC devices and sorting the IC devices in accordance with their automatically read ID codes where the fuse ID either identifies a wafer lot ID, identifies the week the IC's were fabricated, identifies

a wafer ID, identifies a die location on the wafer, and/or identifies a fabrication facility ID. Such are not the elements of the presently claimed inventions of presently amended independent claims 60 and 80 wherein the data stored is based on storing data in association with the ""storing data in association with the identification code of each semiconductor device that identifies manufacturing procedures ~~the~~ each semiconductor device has undergone", "accessing the data stored in association with the identification code associated with the at least one semiconductor device", "storing data in association with the identification code of the at least one semiconductor device identifying manufacturing procedures the at least one semiconductor device has undergone", and "accessing the data stored in association with the identification code associated with the at least two semiconductor devices". In Applicants' claimed inventions, the data in the identification code is based on manufacturing procedures where the cited prior art is not.

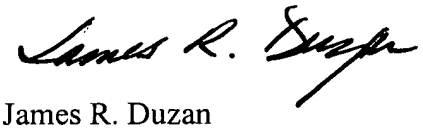
Additionally, Applicants assert that any rejection of the claimed inventions of claims 68 through 72 and 88 through 92 based on any combination of the Beffa reference and the Vu et al. reference under 35 U.S.C. § 103 is a hindsight reconstruction of the Applicants claimed inventions based solely upon Applicants' disclosure because any combination of the cited prior art fail to teach or suggest all the claim limitations of the claimed inventions as well as fails to suggest any combination thereof as set forth herein. Such a rejection is neither within the ambit nor the purview of 35 U.S.C. § 103 and, clearly, improper.

Accordingly, presently amended independent claims 60 and 80 are allowable as well as dependent claims 68 through 72 and 88 through 92 therefrom.

In summary, Applicants submit that claims 1 through 108 are clearly allowable over the cited prior art for the reasons herein.

Applicants request the allowance of claims 1 through 108 and the case passed for issue.

Respectfully submitted,



James R. Duzan
Registration No. 28,393
Attorney for Applicants
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: April 1, 2004
JRD/sls/df/djp

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